What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A sense amplifier control circuit for a memory device comprising:

a first logic gate having a first input coupled to a source of a global control signal, a second input coupled to a source of a first section signal, and an output;

a second logic gate having a first input coupled to said source of said global control signal, a second input coupled to a source of a second section signal, and an output;

a third logic gate having a first input coupled to said source of said global control signal, a second input coupled to said source of said second section signal, and an output;

a fourth logic gate having a first input coupled to said source of said global control signal, a second input coupled to a source of a third section signal, and an output;

said first, second, third and fourth logic gates substantially electrically equidistant from said source of said global control signal;

a fifth logic gate having a first input coupled to said output of said first logic gate, a second input coupled to said output of said second logic gate, and an output coupled to a sense amplifier on a first side of a section of said memory; and

a sixth logic gate having a first input coupled to said output of said third logic gate, a second input coupled to said output of said fourth logic gate, and an output coupled to a sense amplifier on a second side of a section of said memory,

wherein when said global control signal and said second section signal are active, said fifth and sixth logic gates provide a sense amplifier control signal to said sense amplifiers on said first and second sides of said section of said memory, respectively, to activate said sense amplifiers on said first and second sides of said section of said memory substantially simultaneously.

2. The control circuit according to claim 1, further comprising:

a first inverter coupled between said output of said fifth logic gate and said sense amplifier on said first side of said section of said memory; and

a second inverter coupled between said output of said sixth logic gate and said sense amplifier on said second side of said section of said memory.

3. The control circuit according to claim 2, wherein said sense amplifier control signal fires a P-sense amplifier in said sense amplifiers on said first and second sides of said section of said memory.

4. The control circuit according to claim 1, wherein each of said first, second, third, fourth, fifth and sixth logic gates are NAND gates.

5. The control circuit according to claim 1, wherein if said section of said memory is located at an edge of said memory, said first and second input of said first logic gate are coupled to ground.

6. The control circuit according to claim 1, wherein said sense amplifier control signal fires a N-sense amplifier in said sense amplifiers on said first and second sides of said section of said memory.

7. The control circuit according to claim 1, wherein said sense amplifier control signal fires an equilibration circuit in said sense amplifiers on said first and second sides of said section of said memory.

8. The control circuit according to claim 1, wherein said global control signal is input to said second and third logic gates at substantially the same time.

9. A circuit for providing a respective control signal to sense amplifiers located on each side of a plurality of sections of a memory, said circuit comprising:

a first plurality of NAND gates, each of said first plurality of NAND gates having a first input coupled to a source of a global control signal and a second input coupled to a source of a respective section signal, said respective section signal being associated with a respective one of said plurality of sections, each gate of said first plurality of NAND gates substantially electrically equidistant from said source of said global control signal; and

a second plurality of NAND gates, each of said second plurality of NAND gates having a first input coupled to an output of one of said first plurality of NAND gates, a second input coupled to an output of another of said first plurality of NAND gates, and an output coupled to a respective one of said sense amplifiers, said output providing said respective control signal to said respective one of said sense amplifiers.

10. The circuit according to claim 9, further comprising:

a plurality of inverters, each of said inverters having an input coupled to an output of a respective one of said second plurality of NAND gates and an output coupled to said respective one of said sense amplifiers to provide said respective control signal to said respective one of said sense amplifiers.

11. The circuit according to claim 10, wherein said control signal fires a P-sense amplifier in said respective one of said sense amplifiers on each side of one of said sections substantially simultaneously.

12. The circuit according to claim 9, wherein said control signal fires a N-sense amplifier in said respective one of said sense amplifiers on each side of one of said sections substantially simultaneously.

13. The circuit according to claim 9, wherein said control signal fires an equilibration circuit in said respective one of said sense amplifiers on each side of one of said sections substantially simultaneously.

14. The circuit according to claim 9, wherein said global control signal is received by a corresponding pair of said first plurality of NAND gates at substantially the same time.

15. The circuit according to claim 9, wherein said one of said first plurality of NAND gates and said another of said first plurality of NAND gates are equidistant from a respective one of said second plurality of NAND gates.

16. A memory device comprising:

a plurality of sections, each of said plurality of sections including an array of memory cells;

a plurality of rows of sense amplifiers, each of said plurality of rows of sense amplifiers being located between a pair of said plurality of sections; and

a control circuit for providing a respective control signal to each of said plurality of rows of sense amplifiers, said control circuit comprising:

a first plurality of NAND gates, each of said first plurality of NAND gates having a first input coupled to a source of a global control signal and a second input coupled to a source of a respective section signal, said respective section signal being

associated with a respective one of said plurality of sections, each gate of said first plurality of NAND gates substantially electrically equidistant from said source of said global control signal; and

a second plurality of NAND gates, each of said second plurality of NAND gates having a first input coupled to an output of one of said first plurality of NAND gates, a second input coupled to an output of another of said first plurality of NAND gates, and an output coupled to a respective one of said rows of sense amplifiers to provide said respective control signal to said respective one of said rows of sense amplifiers.

17. The memory device according to claim 16, wherein said control circuit further comprises:

a plurality of inverters, each of said inverters having an input coupled to an output of a respective one of said second plurality of NAND gates and an output coupled to said respective one of said rows of sense amplifiers to provide said respective control signal to said respective one of said rows of sense amplifiers.

18. The memory device according to claim 17, wherein said respective control signal fires a P-sense amplifier in said respective one of said rows of sense amplifiers on each side of one of said sections substantially simultaneously.

19. The memory device according to claim 16, wherein said respective control signal fires an N-sense amplifier in said respective one of said rows of sense amplifiers on each side of one of said sections substantially simultaneously.

20. The memory device according to claim 16, wherein said respective control signal fires an equilibration circuit in said respective one of said rows of sense amplifiers on each side of one of said sections substantially simultaneously.

21. The memory device according to claim 16, wherein said global control signal is received by a corresponding pair of said first plurality of NAND gates at substantially the same time.

22. The memory device according to claim 16, wherein said one of said first plurality of NAND gates and said another of said first plurality of NAND gates are equidistant from a respective one of said second plurality of NAND gates.

23. A memory device comprising:

a plurality of sections, each of said plurality of sections including an array of memory cells;

a plurality of rows of sense amplifiers, each of said plurality of rows of sense amplifiers being located between a pair of said plurality of sections; and

a control circuit for providing a respective control signal to each of said plurality of rows of sense amplifiers, said control circuit comprising:

a first logic gate having a first input coupled to a source of a global control signal, a second input coupled to a source of a first section signal associated with a first one of said plurality of sections, and an output;

a second logic gate having a first input coupled to said source of said global control signal, a second input coupled to a source of a second section signal associated with a second one of said plurality of sections, and an output;

a third logic gate having a first input coupled to said source of said global control signal, a second input coupled to said source of said second section signal, and an output;

a fourth logic gate having a first input coupled to said source of said global control signal, a second input coupled to a source of a third section signal associated with third one of said plurality of sections, and an output;

said first, second, third and fourth logic gates substantially electrically equidistant from said source of said global control signal;

a fifth logic gate having a first input coupled to said output of said first logic gate, a second input coupled to said output of said second logic gate, and an output coupled to said row of sense amplifiers located between said first one and said second one of said plurality of sections; and

a sixth logic gate having a first input coupled to said output of said third logic gate, a second input coupled to said output of said fourth logic gate, and an output coupled to said row of sense amplifiers located between said second one and said third one of said plurality of sections,

wherein when said global control signal and said second section signal are active, said fifth and sixth logic gates provide a sense amplifier control signal to said row of sense amplifiers located between said first one and said second one of said plurality of sections and said row of sense amplifiers located between said second one and said third one of said plurality of sections, respectively, to activate said row of sense amplifiers located between said first one and said second one of said plurality of sections and said row of sense amplifiers located between said second one and said third one of said plurality of sections substantially simultaneously.

24. The memory device according to claim 23, said control circuit further comprising:

a first inverter coupled between said output of said fifth logic gate and said row of sense amplifiers located between said first one and said second one of said plurality of sections; and

a second inverter coupled between said output of said sixth logic gate and said row of sense amplifiers located between said second one and said third one of said plurality of sections.

25. The memory device according to claim 24, wherein said respective control signal fires a P-sense amplifier in said sense amplifiers located between said first one and said second one of said plurality of sections and said row of sense amplifiers located between said second one and said third one of said plurality of sections.

26. The memory device according to claim 23, wherein each of said first, second, third, fourth, fifth and sixth logic gates are NAND gates.

27. The memory device according to claim 23, wherein if said first one of said plurality of sections of said memory is located at an edge of said memory, said first and second input of said first logic gate are coupled to ground.

28. The memory device according to claim 23, wherein said respective control signal fires an N-sense amplifier in said row of sense amplifiers located between said first one and said second one of said plurality of sections and said row of sense amplifiers located between said second one and said third one of said plurality of sections.

29. The memory device according to claim 23, wherein said respective control signal fires an equilibration circuit in said row of sense amplifiers located between said first one and said second one of said plurality of sections and said row of sense amplifiers located between said second one and said third one of said plurality of sections.

30. A memory device comprising:

a plurality of arrays;

a plurality of rows of sense amplifiers, each of said plurality of rows of sense amplifiers being between a respective pair of said plurality of arrays; and

a logic circuit for providing a respective control signal to each of said plurality of rows of sense amplifiers, said logic circuit causing said respective control signal to be applied to respective rows of said sense amplifiers on each side of at least one of said plurality of arrays substantially simultaneously.

31. The memory device according to claim 30, wherein said logic circuit comprises a plurality of NAND gates coupled in an equidistant tree circuit.

32. The memory device according to claim 30, wherein said logic circuit further comprises:

a first plurality of NAND gates, each of said first plurality of NAND gates having a first input coupled to a source of a global control signal and a second input coupled to a source of a respective section signal, said respective section signal being associated with a respective one of said plurality of arrays, each gate of said first plurality of NAND gates substantially electrically equidistant from said source of said global control signal; and

a second plurality of NAND gates, each of said second plurality of NAND gates having a first input coupled to an output of one of said first plurality of NAND

gates, a second signal input coupled to an output of another of said first plurality of NAND gates, and an output coupled to a respective one of said rows of sense amplifiers to provide said respective control signal to said respective rows of said sense amplifiers on each side of said at least one of said plurality of arrays

33. The memory device according to claim 32, wherein said logic circuit further comprises:

a plurality of inverters, each of said inverters having an input coupled to an output of a respective one of said second plurality of NAND gates and an output coupled to said respective one of said rows of sense amplifiers to provide said respective control signal to said respective rows of said sense amplifiers on each side of said at least one of said plurality of arrays.

34. The memory device according to claim 33, wherein said respective control signal fires a P-sense amplifier in said respective rows of said sense amplifier on each side of said at least one of said plurality of arrays.

35. The memory device according to claim 30, wherein in response to said respective control signal, a P-sense amplifier in said respective row is activated.

36. The memory device according to claim 30, wherein in response to said respective control signal, an N-sense amplifier in said respective row is activated.

37. The memory device according to claim 36, wherein in response to said respective control signal, an equilibration circuit in said respective row is activated.

38. A processor system comprising:

a processing unit; and

a memory device connected to said processing unit, said memory device comprising:

a plurality of sections, each of said plurality of sections including an array of memory cells;

a plurality of rows of sense amplifiers, each of said plurality of rows of sense amplifiers being located between a pair of said plurality of sections; and

a control circuit for providing a respective control signal to each of said plurality of rows of sense amplifiers, said control circuit comprising:

a first plurality of NAND gates, each of said first plurality of NAND gates having a first input coupled to a source of a global control signal and a second input coupled to a source of a respective section signal, said respective section signal being associated with a respective one of said plurality of sections, each gate of said first plurality of NAND gates substantially electrically equidistant from said source of said global control signal; and

a second plurality of NAND gates, each of said second plurality of NAND gates having a first input coupled to an output of one of said first plurality of NAND gates, a second input coupled to an output of another of said first plurality of NAND gates, and an output coupled to a respective one of said rows of sense amplifiers to provide said respective control signal to said respective one of said rows of sense amplifiers.

39. The processor system according to claim 38, wherein said control circuit further comprises:

a plurality of inverters, each of said inverters having an input coupled to an output of a respective one of said second plurality of NAND gates and an output coupled to said respective one of said rows of sense amplifiers to provide said respective control signal to said respective one of said rows of sense amplifiers.

40. The processor system according to claim 39, wherein said respective control signal fires a P-sense amplifier in said respective one of said rows of sense amplifiers on each side of one of said sections substantially simultaneously.

41. The processor system according to claim 38, wherein said respective control signal fires an N-sense amplifier in said respective one of said rows of sense amplifiers on each side of one of said sections substantially simultaneously.

42. The processor system according to claim 38, wherein said respective control signal fires an equilibration circuit in said respective one of said rows of sense amplifiers on each side of one of said sections substantially simultaneously.

43. The processor system according to claim 38, wherein said processing unit and said memory device are on a same chip.

44. The processor system according to claim 38, wherein said global control signal is received by a corresponding pair of said first plurality of NAND gates at substantially the same time.

45. The processor system according to claim 38, wherein said one of said first plurality of NAND gates and said another of said first plurality of NAND gates are equidistant from a respective one of said second plurality of NAND gates.

46. A processor system comprising:

a processing unit; and

a memory device connected to said processing unit, said memory device comprising:

a plurality of sections, each of said plurality of sections including an array of memory cells;

a plurality of rows of sense amplifiers, each of said plurality of rows of sense amplifiers being located between a pair of said plurality of sections; and

a control circuit for providing a respective control signal to each of said plurality of rows of sense amplifiers, said control circuit comprising:

a first logic gate having a first input coupled to a source of a global control signal, a second input coupled to a source of a first section signal associated with a first one of said plurality of sections, and an output;

a second logic gate having a first input coupled to said source of said global control signal, a second input coupled to a second section signal associated with a second one of said plurality of sections, and an output;

a third logic gate having a first input coupled to said source of said global control signal, a second input coupled to said source of said second section signal, and an output;

a fourth logic gate having a first input coupled to said source of said global control signal, a second input coupled to a source of a third section signal associated with third one of said plurality of sections, and an output;

said first, second, third and fourth logic gates substantially electrically equidistant from said source of said global control signal;

a fifth logic gate having a first input coupled to said output of said first logic gate, a second input coupled to said output of said second logic gate, and an output coupled to said row of sense amplifiers located between said first one and said second one of said plurality of sections; and

a sixth logic gate having a first input coupled to said output of said third logic gate, a second input coupled to said output of said fourth logic gate, and an output coupled to said row of sense amplifiers located between said second one and said third one of said plurality of sections,

wherein when said global control signal and said second section signal are active, said fifth and sixth logic gates provide a sense amplifier control signal to said row of sense amplifiers located between said first one and said second one of said plurality of sections and said row of sense amplifiers located between said second one and said third one of said plurality of sections, respectively, to activate said row of sense amplifiers located between said first one and said second one of said plurality of sections and said row of sense amplifiers located between said second one and said third one of said plurality of sections substantially simultaneously.

47. The processor system according to claim 46, said control circuit further comprising:

a first inverter coupled between said output of said fifth logic gate and said row of sense amplifiers located between said first one and said second one of said plurality of sections; and

a second inverter coupled between said output of said sixth logic gate and said row of sense amplifiers located between said second one and said third one of said plurality of sections.

48. The processor system according to claim 47, wherein said respective control signal fires a P-sense amplifier in said sense amplifiers located between said first one and said second one of said plurality of sections and said row of sense amplifiers located between said second one and said third one of said plurality of sections.

49. The processor system according to claim 46, wherein each of said first, second, third, fourth, fifth and sixth logic gates are NAND gates.

50. The processor system according to claim 46, wherein if said first one of said plurality of sections of said memory is located at an edge of said memory, said first and second input of said first logic gate are coupled to ground.

51. The processor system according to claim 46, wherein said respective control signal fires an N-sense amplifier in said row of sense amplifiers located between said first one and said second one of said plurality of sections and said row of sense amplifiers located between said second one and said third one of said plurality of sections.

52. The processor system according to claim 46, wherein said respective control signal fires an equilibration circuit in said row of sense amplifiers located between said first one and said second one of said plurality of sections and said row of sense

amplifiers located between said second one and said third one of said plurality of sections.

53. A processor system comprising:

a processing unit; and

a memory device connected to said processing unit, said memory comprising:

a plurality of arrays;

a plurality of rows of sense amplifiers, each of said plurality of rows of sense amplifiers being between a respective pair of said plurality of arrays; and

a logic circuit for providing a repetitive control signal to each of said plurality of rows of sense amplifiers, said logic circuit causing solid respective control signals to be applied to respective rows of said sense amplifiers on each side of at least one of said plurality of array substantially simultaneously.

54. The processor system according to claim 53, wherein said logic circuit comprises a plurality of NAND gates coupled in a tree circuit.

55. The processor system according to claim 53, wherein said logic circuit further comprises:

a first plurality of NAND gates, each of said first plurality of NAND gates having a first input coupled to a source of a global control signal and a second input

coupled to a source of a respective section signal, said respective section signal being associated with a respective one of said plurality of arrays, each gate of said first plurality of NAND gates substantially electrically equidistant from said source of said global control signal; and

a second plurality of NAND gates, each of said second plurality of NAND gates having a first input coupled to an output of one of said first plurality of NAND gates, a second signal input coupled to an output of another of said first plurality of NAND gates, and an output coupled to a respective one of said rows of sense amplifier to provide said respective control signal to said respective rows of said sense amplifier on each side of said at least one of said plurality of arrays

56. The processor system according to claim 55, wherein said logic circuit further comprises:

a plurality of inverters, each of said inverters having an input coupled to an output of a respective one of said second plurality of NAND gates and an output coupled to said respective one of said rows of sense amplifiers to provide said respective control signal to said respective rows of said sense amplifiers on each side of said at least one of said plurality of arrays.

57. The processor system according to claim 56, wherein said respective control signal fires a P-sense amplifier in said respective rows of said sense amplifier on each side of said at least one of said plurality of arrays.

58. The processor system according to claim 53, wherein in response to said respective control signal, a P-sense amplifier in said respective row is activated.

59. The processor system according to claim 53, wherein in response to said respective control signal, an N-sense amplifier in said respective row is activated.

60. The processor system according to claim 53, wherein in response to said respective control signal, an equilibration circuit in said respective row is activated.

61. The processor system according to claim 53, wherein said processing unit and said memory device are on a same chip.

62. A method for firing sense amplifiers on a first and second side of a section of a memory, said method comprising:

inputting a global control signal to a first input of a first plurality of logic gates substantially simultaneously;

inputting a respective section signal to a second input of each of said first plurality of logic gates, said respective section signal being associated with said section of said memory;

inputting an output from a first of said first plurality of logic gates to a first input of a first one of a second plurality of logic gates;

inputting an output from a second of said first plurality of logic gates to a second input of said first one of said second plurality of logic gates;

inputting an output from a third of said first plurality of logic gates to a first input of a second one of said second plurality of logic gates;

inputting an output from a fourth of said first plurality of logic gates to a second input of said second one of said second plurality of logic gates; and

providing an output of said first one of said second plurality of logic gates to said sense amplifiers on said first side of said section of said memory and an output of said second one of said second plurality of logic gates to said sense amplifiers on said second side of said section of said memory, said sense amplifiers firing in response to said outputs.

63. The method according to claim 62, further comprising the step of:

providing said output of said first one of said second plurality of logic gates to an input of a first inverter and said output of said second one of said second plurality of logic gates to an input of a second inverter; and

providing an output of said first inverter to said sense amplifiers on said first side of said section of said memory and an output of said second inverter to said sense amplifiers on said second side of said section of said memory, said sense amplifiers firing in response to said outputs of said inverters.

64. The method according to claim 63, wherein said firing of said sense amplifiers further comprises:

firing a P-sense amplifier in said sense amplifiers on said first and second side of said section of said memory.

65. The method according to claim 62, wherein said firing of said sense amplifiers further comprises:

firing an N-sense amplifier in said sense amplifiers on said first and second side of said section of said memory.

66. The method according to claim 62, wherein said firing of said sense amplifiers further comprises:

firing an equilibration circuit in said sense amplifiers on said first and second side of said section of said memory.

67. The method according to claim 62, wherein said firing of said sense amplifiers further comprises:

firing said sense amplifiers on said first and second side of said section of said memory substantially simultaneously.

68. A method for providing a control signal to sense amplifiers located on each side of an array of a memory device, said method comprising:

providing a global signal to a logic circuit;

providing a section signal to said logic circuit, said section signal being associated with said array;

determining an output signal for said logic circuit to output to said sense amplifiers, said output signal being based on said global signal and said section signal; and

providing said output signal as said control signal to said sense amplifiers on each side of said array substantially simultaneously.

69. The method according to claim 68, wherein said logic circuit comprises a plurality of NAND gates.

70. The method according to claim 69, wherein said logic circuit further comprises a plurality of inverters.

71. The method according to claim 68, wherein said control signal causes a P-sense amplifier in said sense amplifiers to activate.

72. The method according to claim 68, wherein said control signal causes an N-sense amplifier in said sense amplifiers to activate.

73. The method according to claim 68, wherein said control signal causes an equilibration circuit in said sense amplifiers to activate.